TER-005

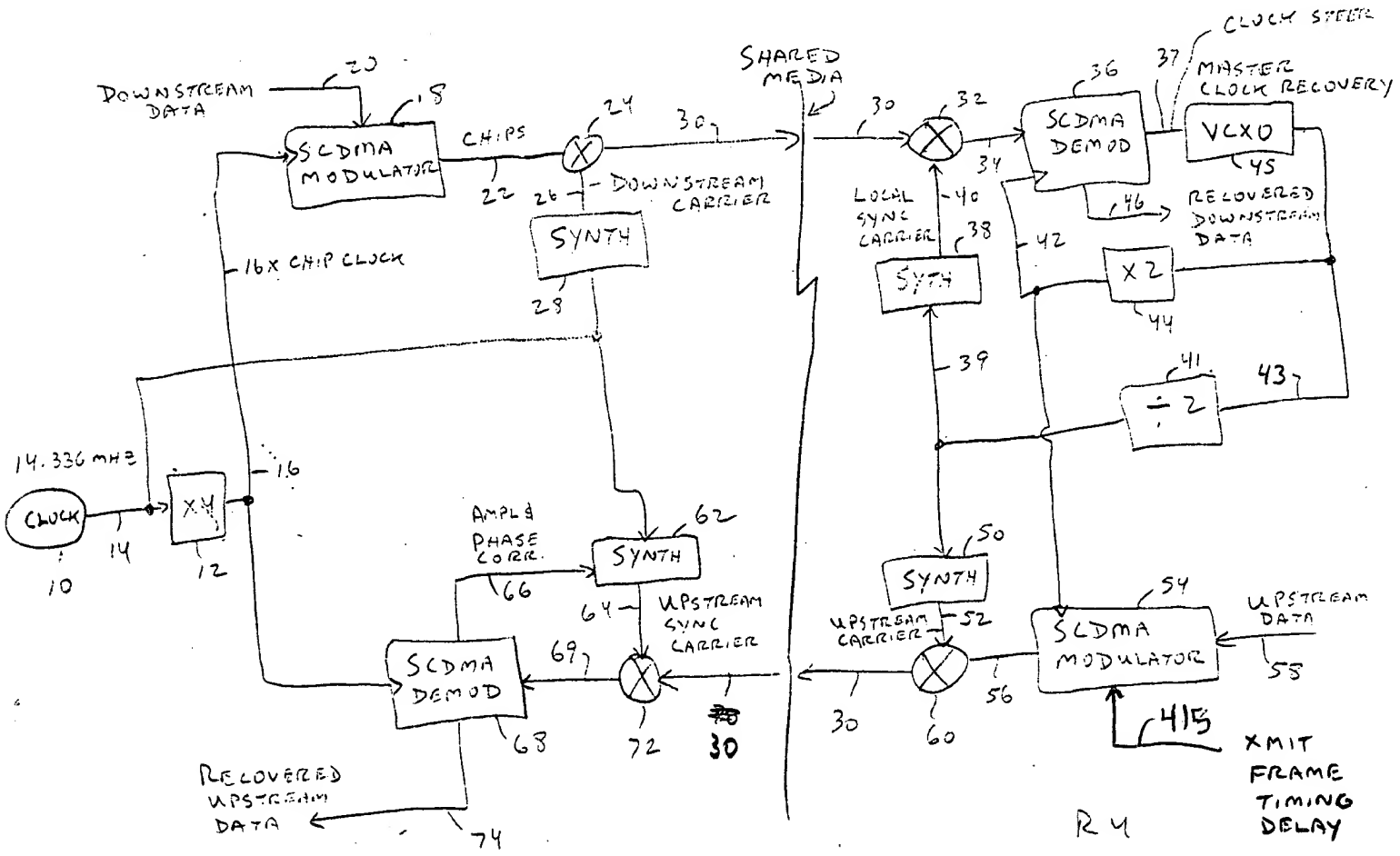


FIG. 1

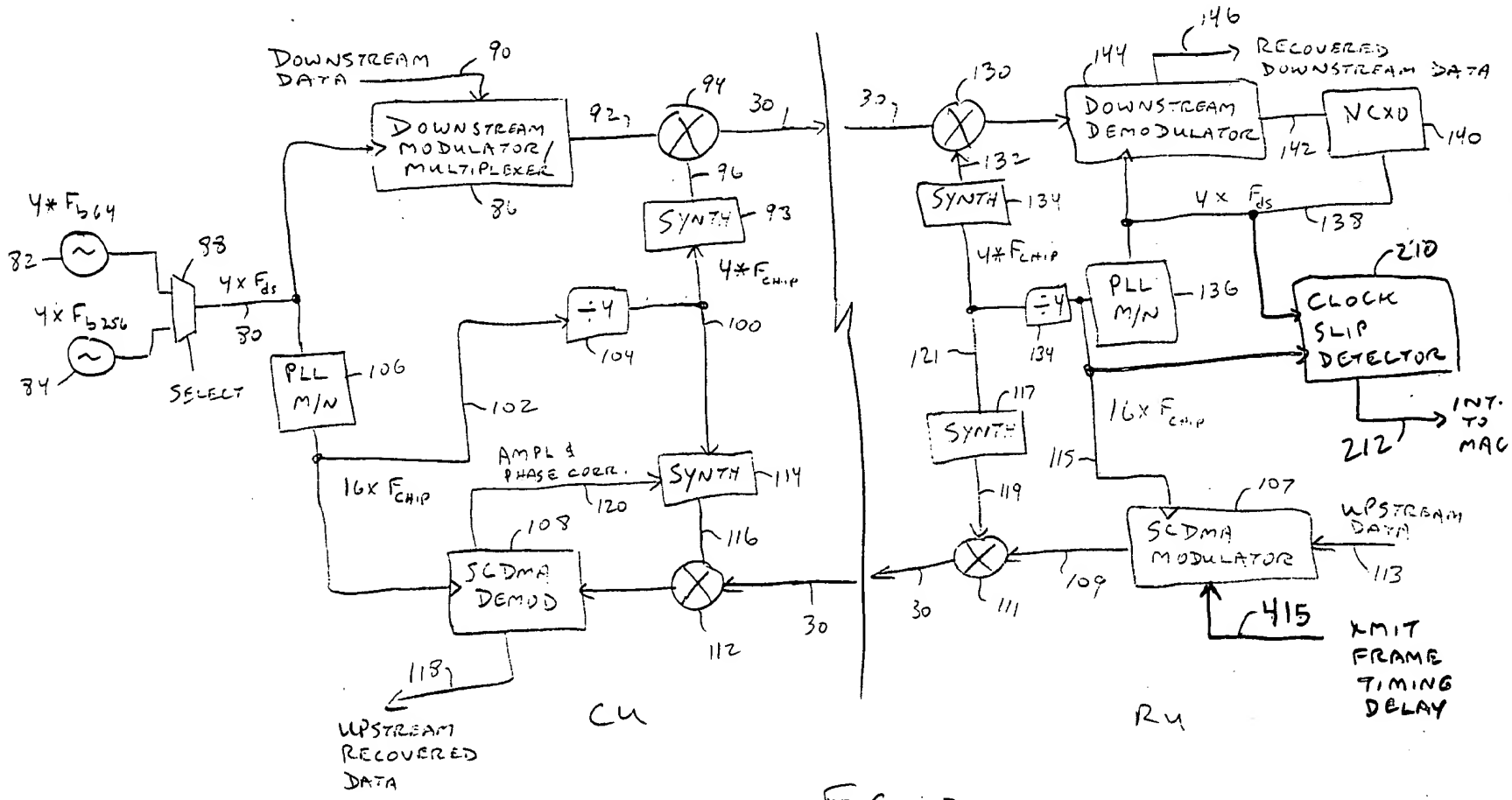


FIG. 2

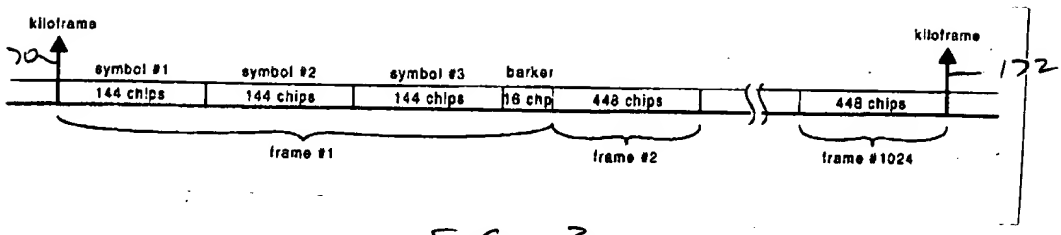


FIG. 3

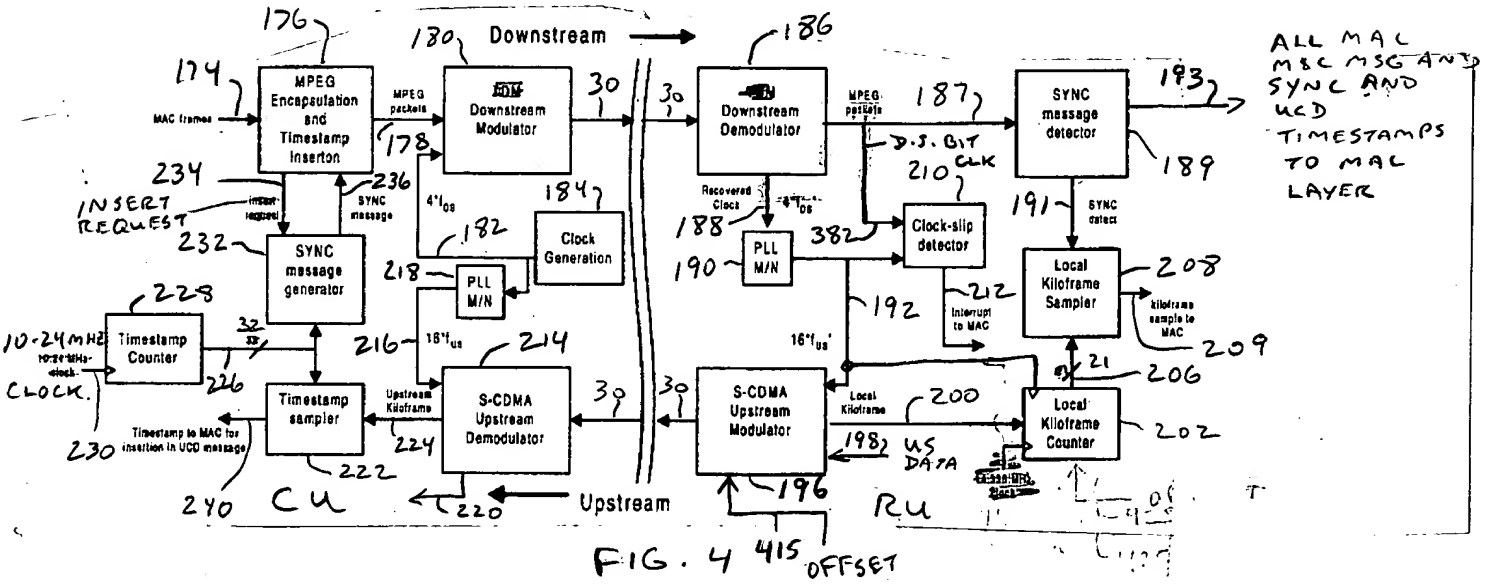
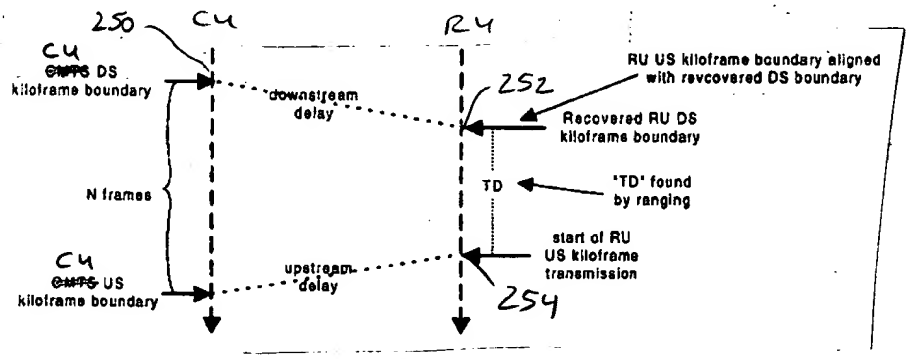


FIG. 4



SCDMA DS, SCDMA US

FIG. 5

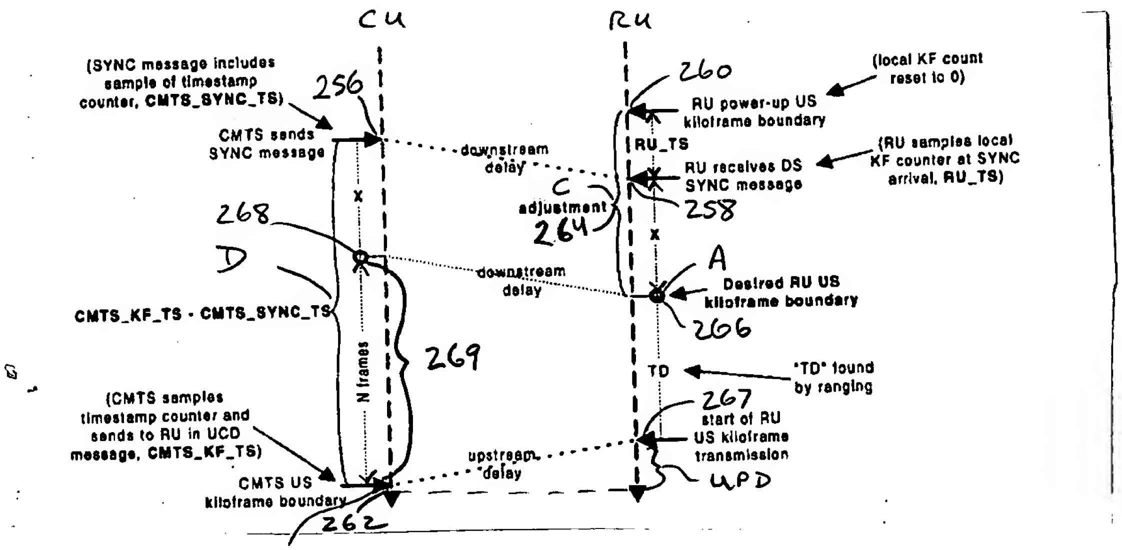

CU
RU
(SYNC message includes sample of timestamp counter, CMTS_SYNC_TS)
256
CMTS sends SYNC message
downstream delay
260
RU power-up US kiloframe boundary
(local KF count reset to 0)
RU_TS
RU receives DS SYNC message
(RU samples local KF counter at SYNC arrival, RU_TS)
C
adjustment
264
258
268
D
x
downstream delay
A
Desired RU US kiloframe boundary
266
CMTS_KF_TS - CMTS_SYNC_TS
N frames
269
TD
"TD" found by ranging
(CMTS samples timestamp counter and sends to RU in UCD message, CMTS_KF_TS)
267
start of RU US kiloframe transmission
upstream delay
UPD
CMTS US kiloframe boundary
262
B

FIG. 6

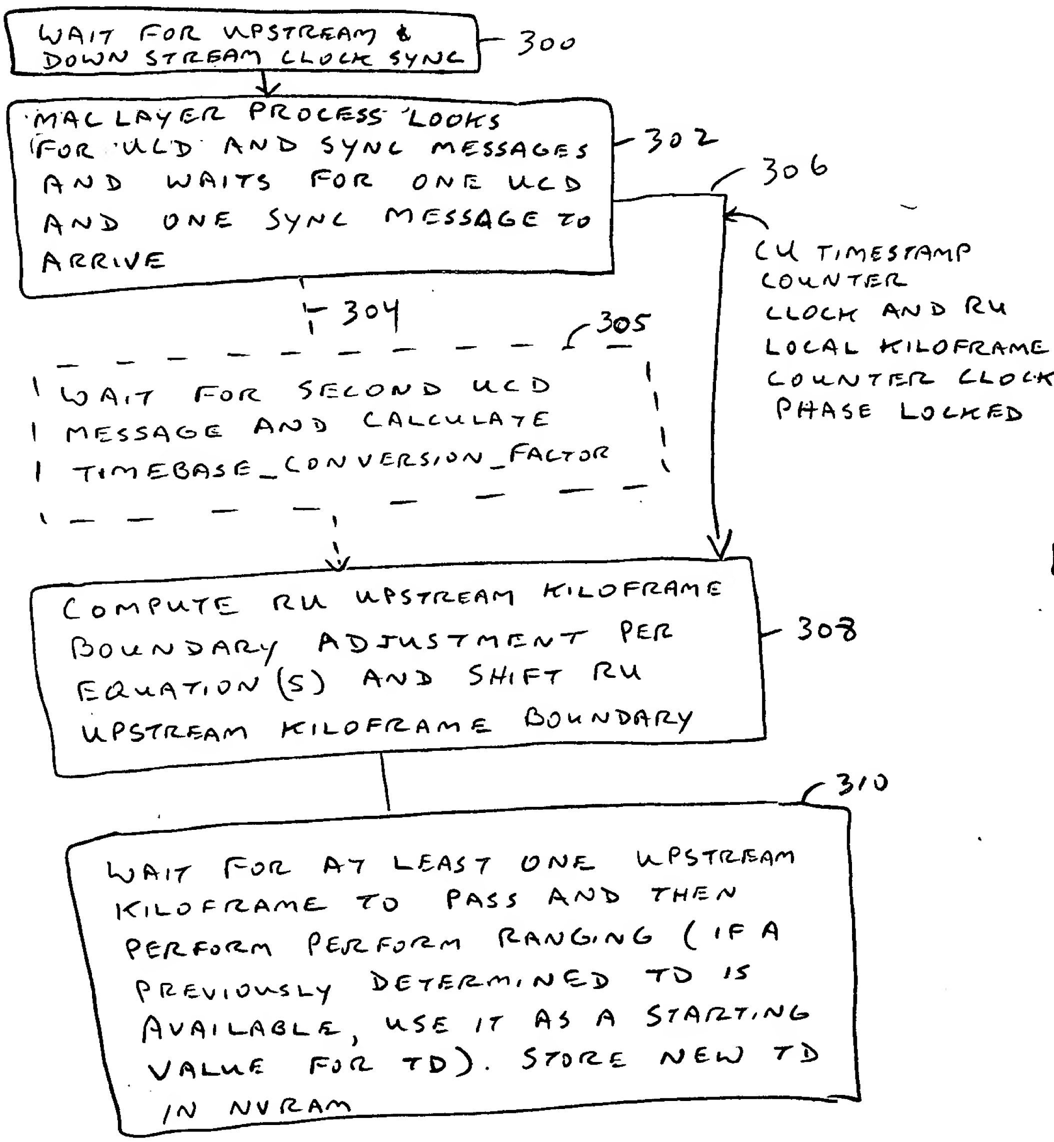

WAIT FOR UPSTREAM & DOWN STREAM CLOCK SYNC
300
MAC LAYER PROCESS LOOKS FOR UCD AND SYNC MESSAGES AND WAITS FOR ONE UCD AND ONE SYNC MESSAGE TO ARRIVE
302
306
CU TIMESTAMP COUNTER CLOCK AND RU LOCAL KILOFRAME COUNTER CLOCK PHASE LOCKED
304
305
WAIT FOR SECOND UCD MESSAGE AND CALCULATE TIMEBASE_CONVERSION_FACTOR
COMPUTE RU UPSTREAM KILOFRAME BOUNDARY ADJUSTMENT PER EQUATION(S) AND SHIFT RU UPSTREAM KILOFRAME BOUNDARY
308
310
WAIT FOR AT LEAST ONE UPSTREAM KILOFRAME TO PASS AND THEN PERFORM PERFORM RANGING (IF A PREVIOUSLY DETERMINED TD IS AVAILABLE, USE IT AS A STARTING VALUE FOR TD). STORE NEW TD IN NVRAM

FIG. 7

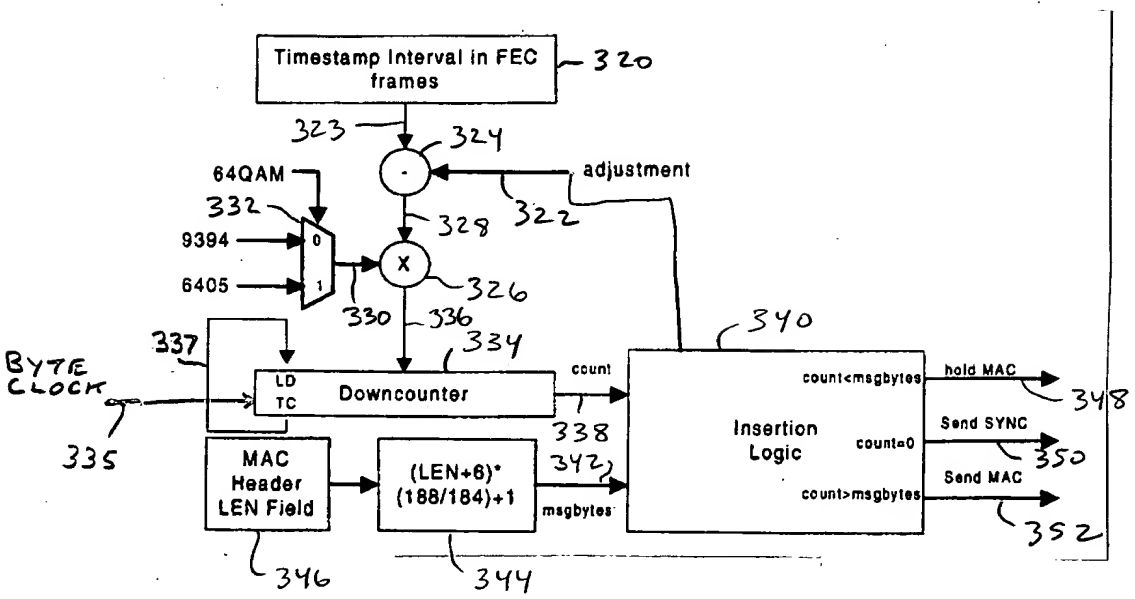


FIG. 8

Table 1 64 QAM SYNC Start Position Adjustments

SYNC Start Position in Bytes	SYNC Adjustment in FEC frames
0-5	2
155-167	4
167-183	2

FIG. 9

Table 2 256 QAM SYNC Start Position Adjustments

SYNC Start Position in Bytes	SYNC Adjustment in FEC frames
0-2	6
3-5	7
155-160	1
161-166	2
167-172	3
173-178	4
179-184	5
185-187	6

FIG. 10

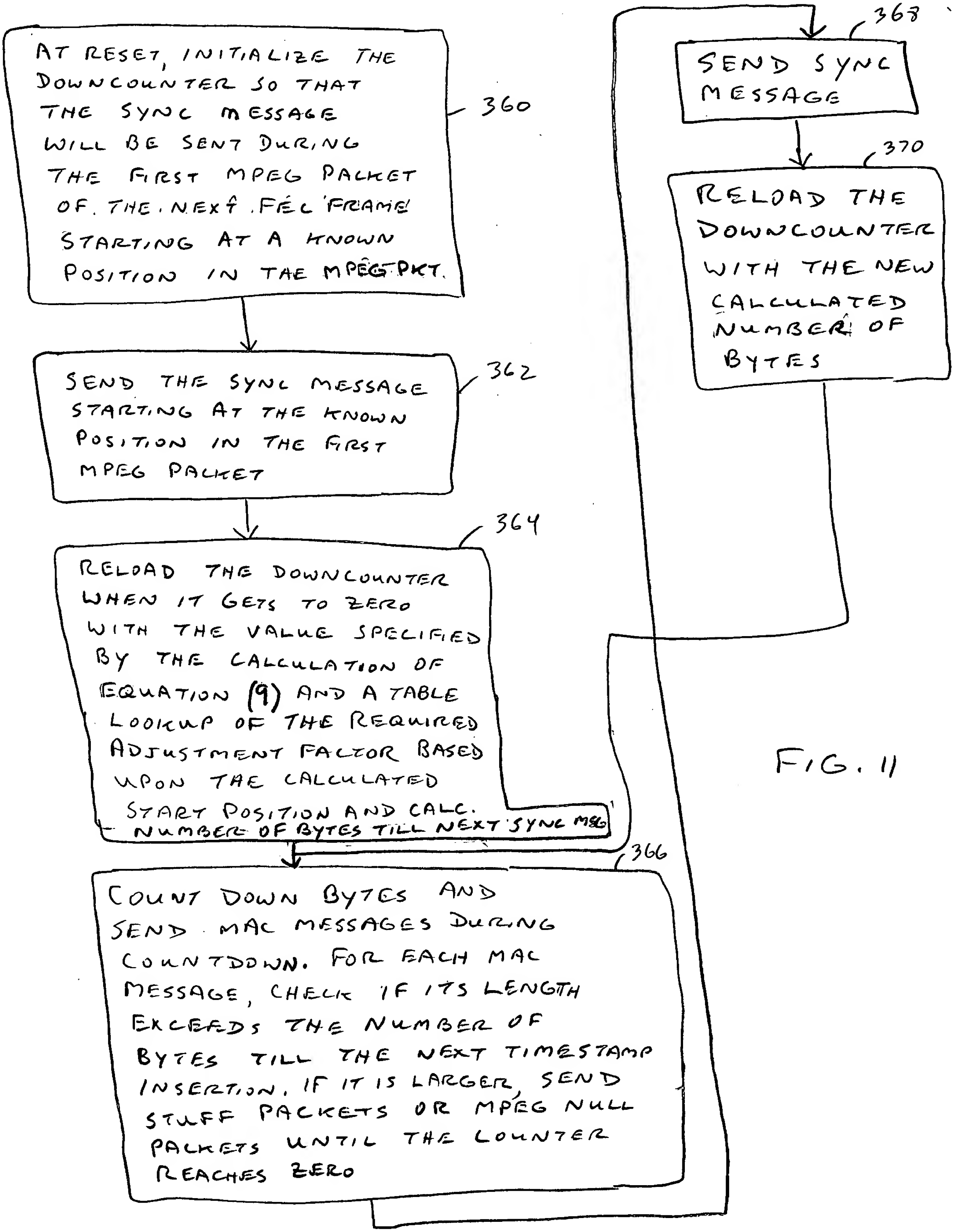


FIG. 11

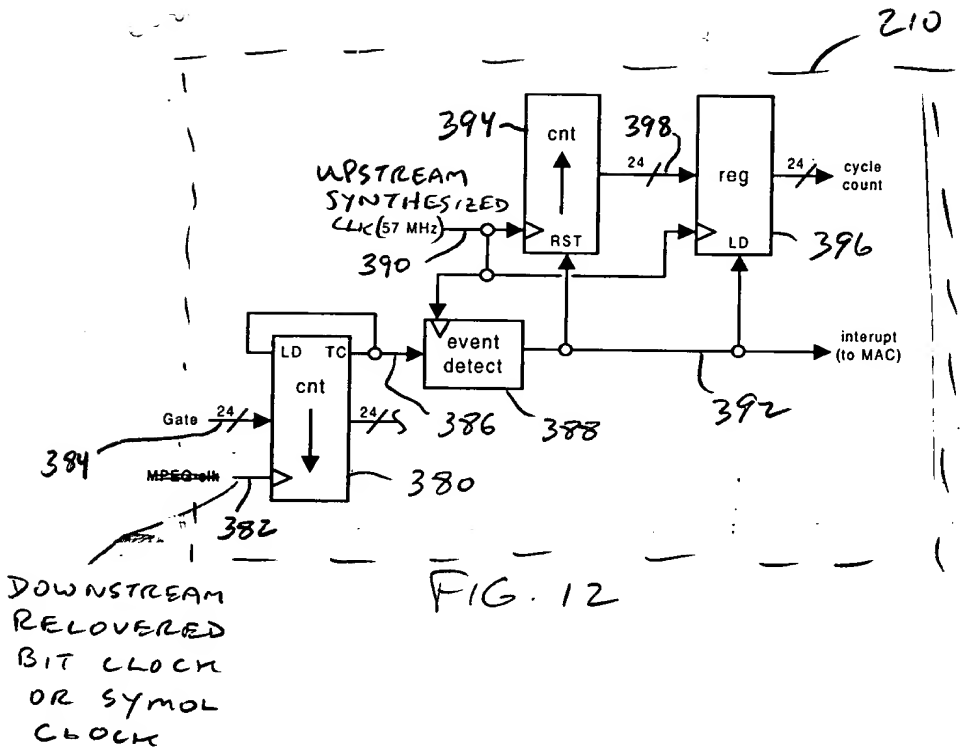

210
394
cnt
398
24
reg
24
cycle count
UPSTREAM SYNTHESIZED CLK (57 MHz)
RST
LD
396
390
LD TC
cnt
event detect
interupt (to MAC)
Gate
24
24
386
388
392
384
MPEG clk
380
382
DOWNSTREAM RECOVERED BIT CLOCK OR SYMOL CLOCK

FIG. 12

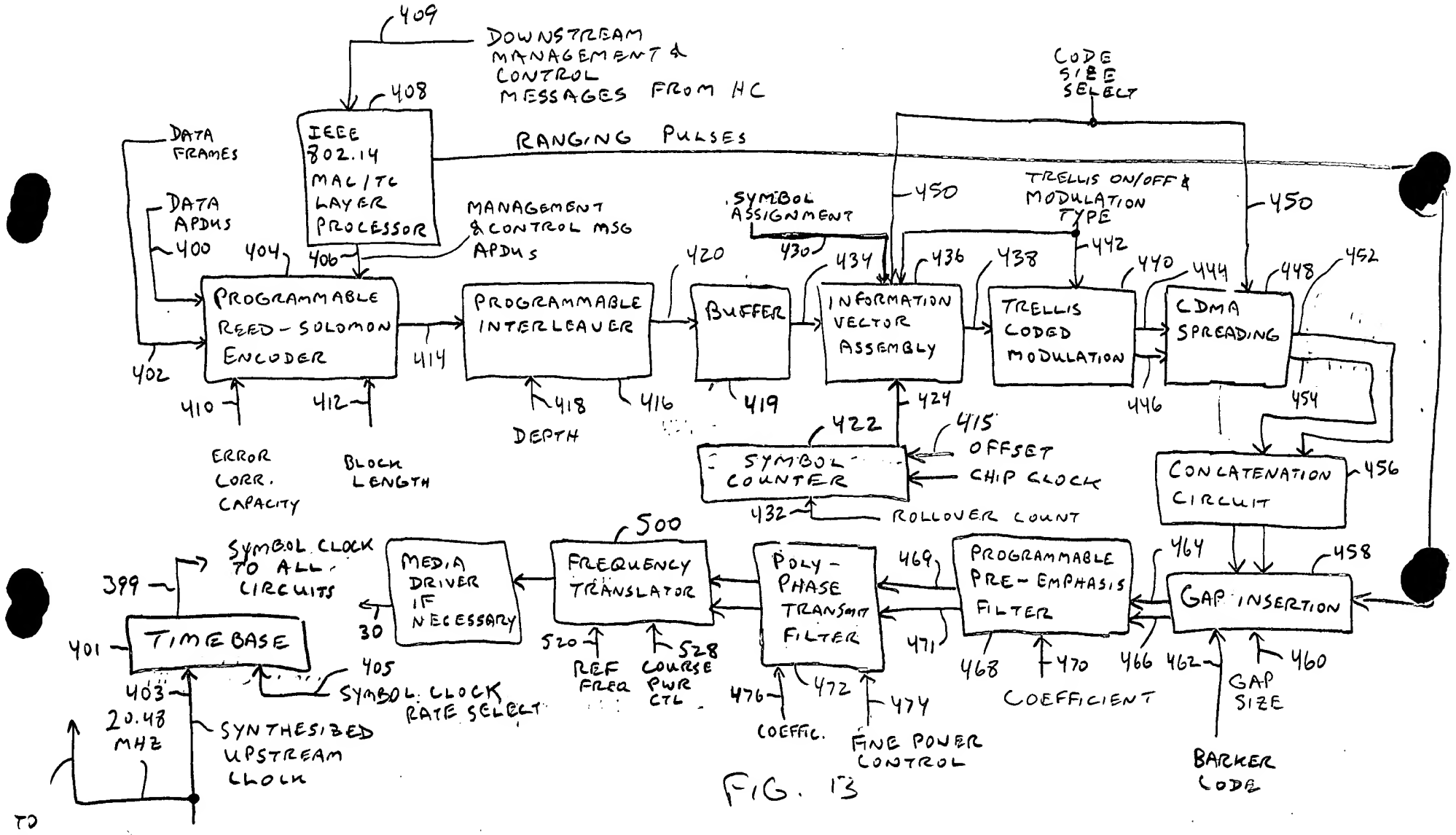
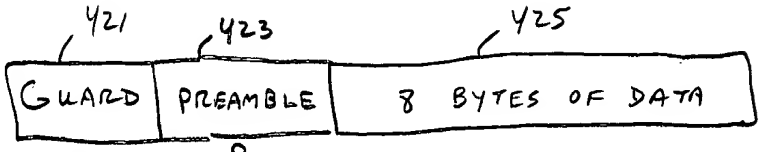
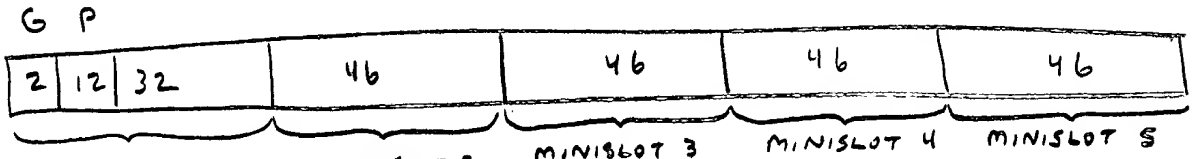

409
DOWNSTREAM MANAGEMENT & CONTROL MESSAGES FROM HC
408
IEEE 802.14 MAC/TC LAYER PROCESSOR
DATA FRAMES
DATA APDUs
400
404
406
MANAGEMENT & CONTROL MSG APDUs
CODE SIZE SELECT
RANGING PULSES
SYMBOL ASSIGNMENT
430
450
TRELLIS ON/OFF & MODULATION TYPE
442
420
434
436
438
440
444
448
452
PROGRAMMABLE REED-SOLOMON ENCODER
PROGRAMMABLE INTERLEAVER
BUFFER
INFORMATION VECTOR ASSEMBLY
TRELLIS CODED MODULATION
CDMA SPREADING
402
414
410
412
418
416
419
424
446
454
ERROR CORR. CAPACITY
BLOCK LENGTH
DEPTH
422
415
SYMBOL COUNTER
OFFSET
CHIP CLOCK
ROLLOVER COUNT
432
CONCATENATION CIRCUIT
456
500
SYMBOL CLOCK TO ALL CIRCUITS
399
MEDIA DRIVER IF NECESSARY
FREQUENCY TRANSLATOR
POLY-PHASE TRANSMIT FILTER
469
PROGRAMMABLE PRE-EMPHASIS FILTER
464
458
GAP INSERTION
401
TIMEBASE
30
520
528
REF FREQ
COURSE PWR CTL
471
468
470
466
462
460
405
403
SYMBOL CLOCK RATE SELECT
476
472
474
COEFFIC.
FINE POWER CONTROL
COEFFICIENT
GAP SIZE
20.48 MHZ
SYNTHESIZED UPSTREAM CLOCK
BARKER CODE
TO CIRCUITS THAT NEED THE MASTER CLOCK TICK RATE

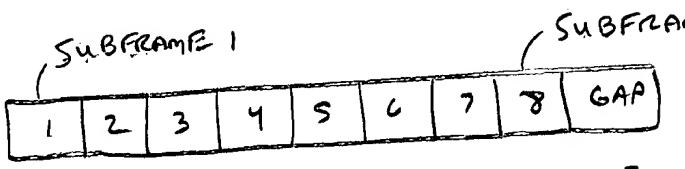
FIG. 13



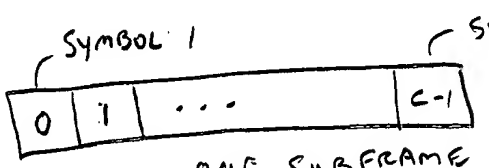
FIRST MINISLOT
FIG. 14



QPSK, NO TRELLIS, 54 BYTE APDU
FIG. 15

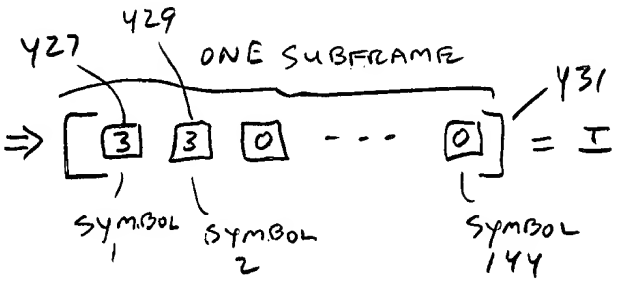


ONE HS-CDMA FRAME
FIG. 16



ONE SUBFRAME
FIG. 17

FIG. 18A CREATE INFORMATION VECTOR = ONE SYMBOL



ONLY CODES 1 & 2 ASSIGNED FOR MINISLOT IN WHICH THIS SYMBOL WILL BE SENT

FIG. 18B TRELLIS ENCODE INFORMATION VECTOR

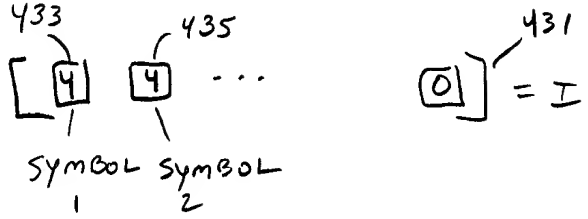
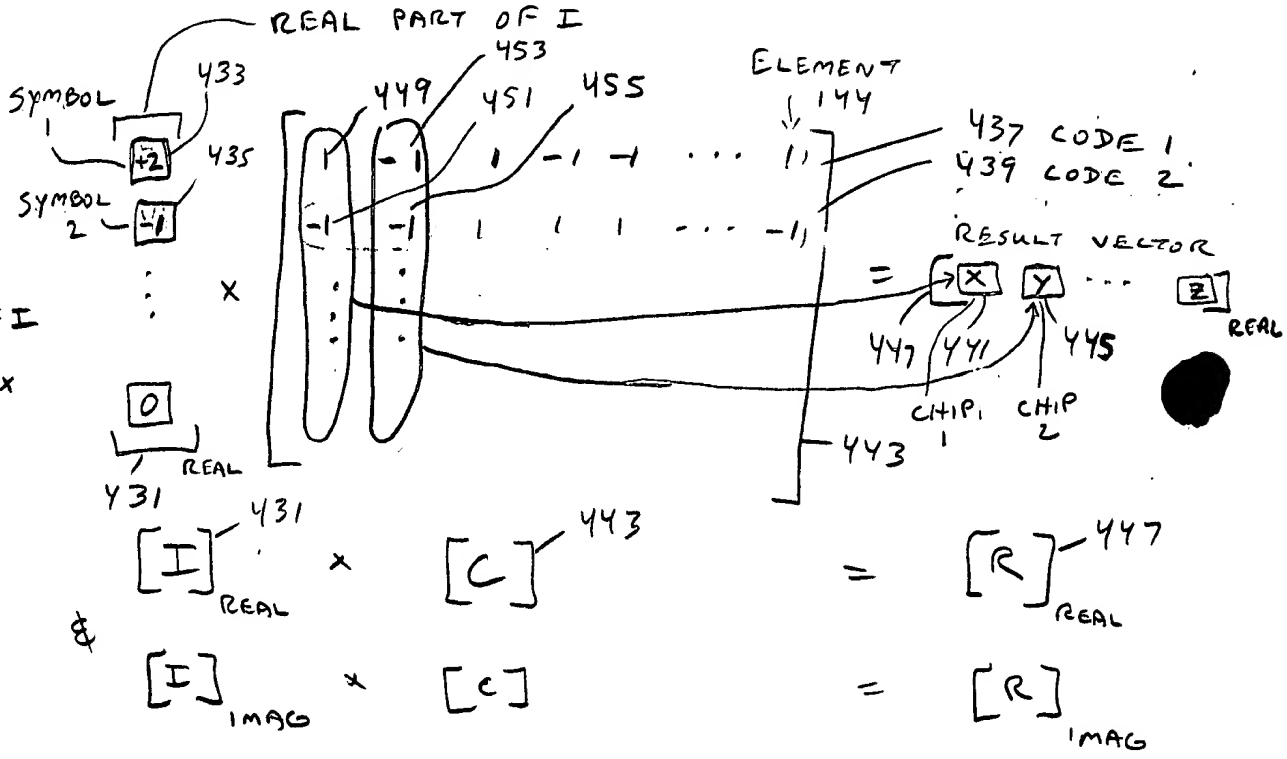


FIG. 18C SPREAD SPECTRUM OF TRELLIS ENCODED INFORMATION VECTOR BY MATRIX MULT. OF I TIMES CODE MATRIX



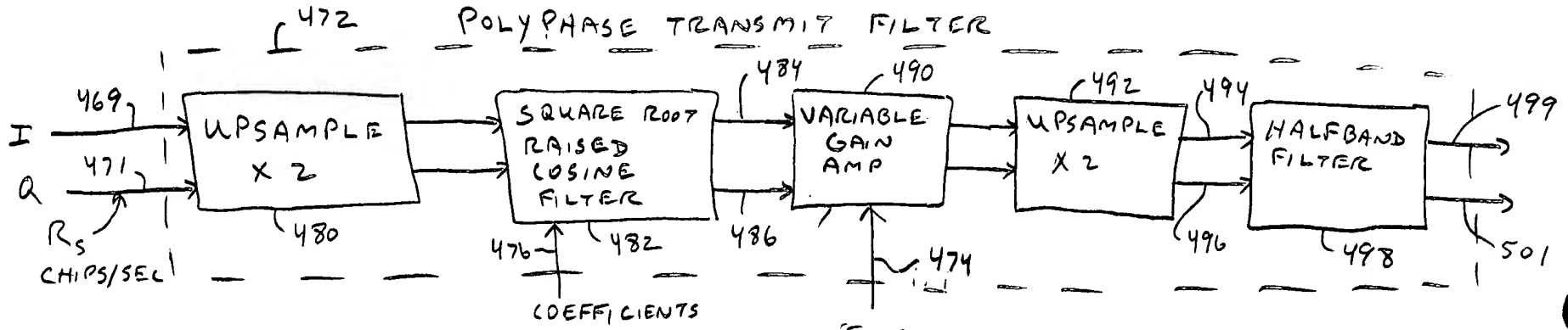


FIG. 19

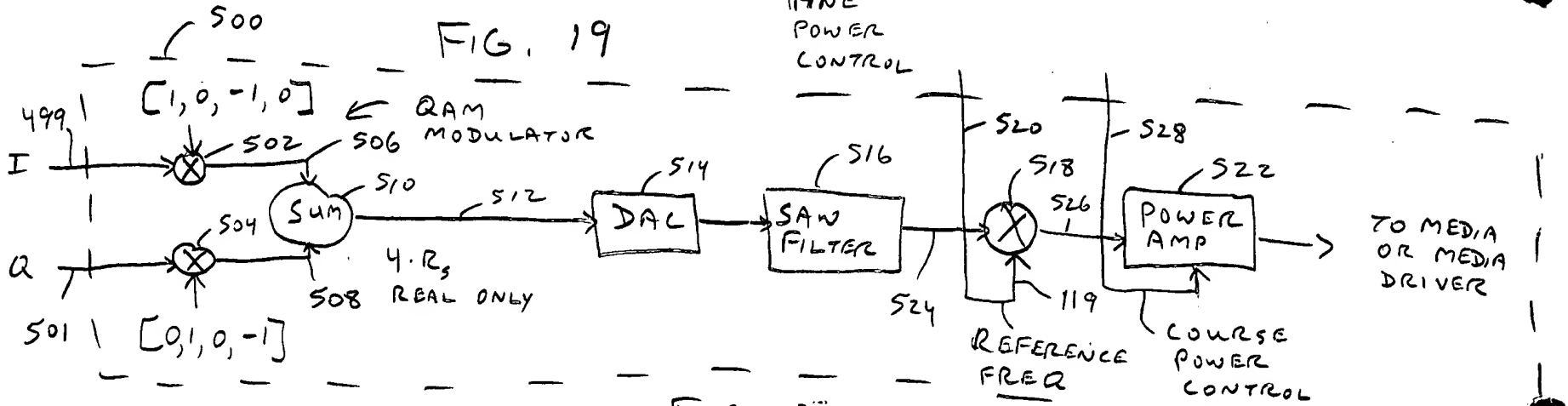


FIG. 20

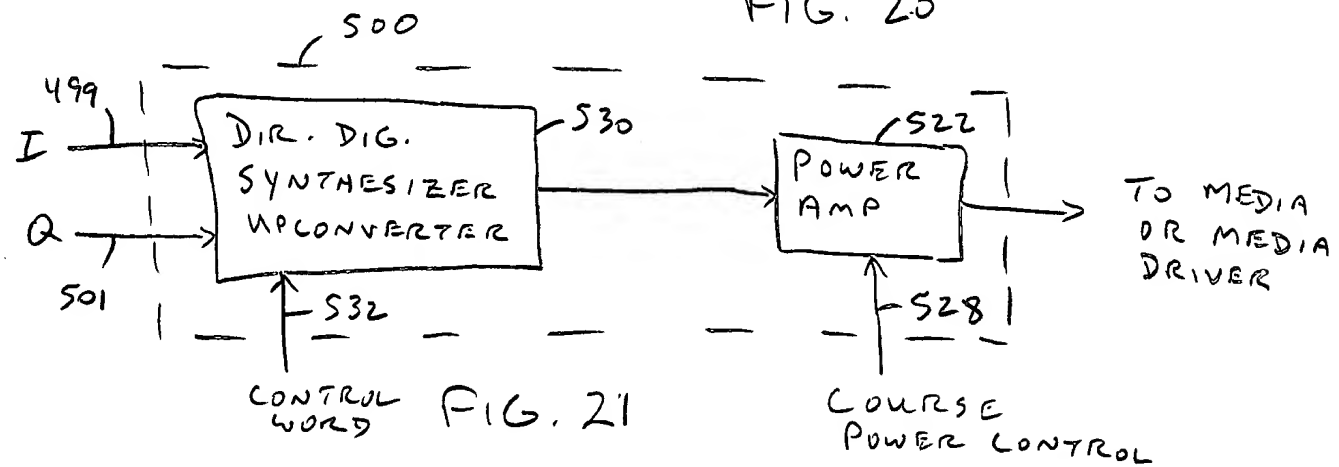


FIG. 21

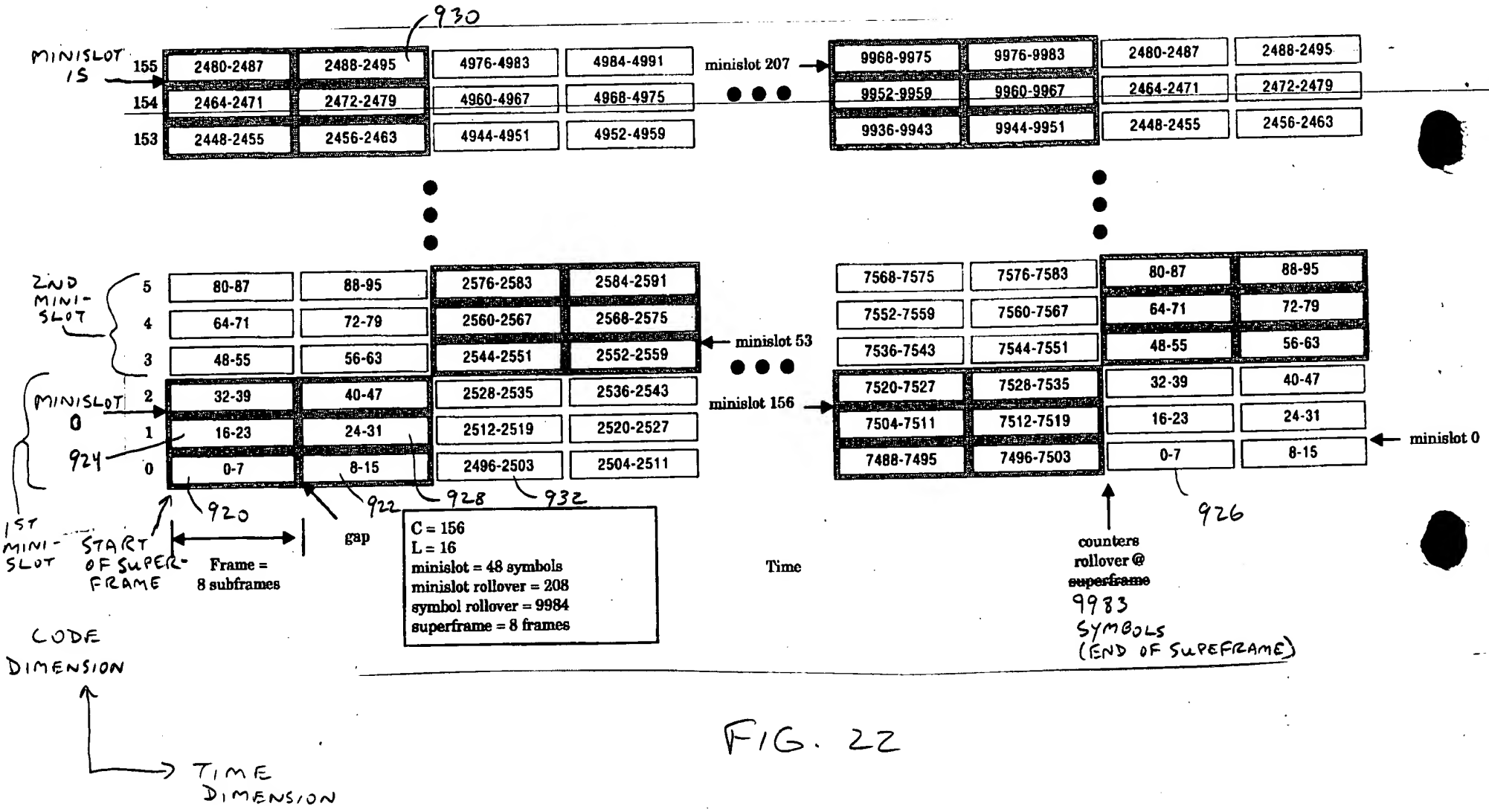

930
MINISLOT IS
155
154
153
2480-2487
2488-2495
4976-4983
4984-4991
2464-2471
2472-2479
4960-4967
4968-4975
2448-2455
2456-2463
4944-4951
4952-4959
minislot 207
9968-9975
9976-9983
2480-2487
2488-2495
9952-9959
9960-9967
2464-2471
2472-2479
9936-9943
9944-9951
2448-2455
2456-2463
2ND MINI-SLOT
5
4
3
80-87
88-95
64-71
72-79
48-55
56-63
2576-2583
2584-2591
2560-2567
2568-2575
2544-2551
2552-2559
minislot 53
7568-7575
7576-7583
7552-7559
7560-7567
7536-7543
7544-7551
80-87
88-95
64-71
72-79
48-55
56-63
MINISLOT 0
924
2
1
0
32-39
40-47
16-23
24-31
0-7
8-15
2528-2535
2536-2543
2512-2519
2520-2527
2496-2503
2504-2511
minislot 156
7520-7527
7528-7535
7504-7511
7512-7519
7488-7495
7496-7503
32-39
40-47
16-23
24-31
0-7
8-15
minislot 0
920
922
928
932
926
1ST MINI-SLOT
START OF SUPER-FRAME
Frame = 8 subframes
gap
C = 156
L = 16
minislot = 48 symbols
minislot rollover = 208
symbol rollover = 9984
superframe = 8 frames
Time
counters rollover @ superframe
9983 SYMBOLS (END OF SUPEFRAME)
CODE DIMENSION
TIME DIMENSION

FIG. 22

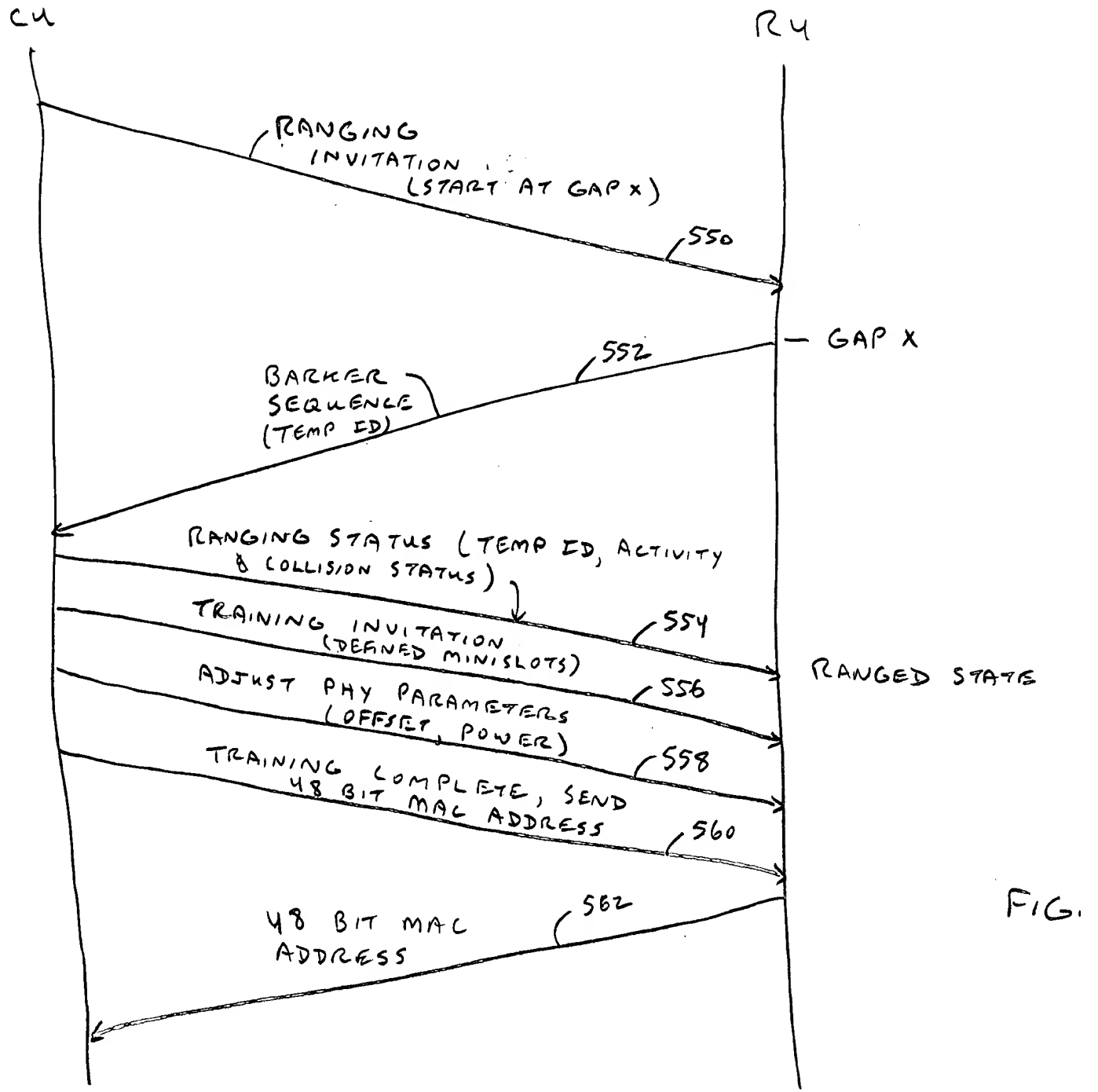
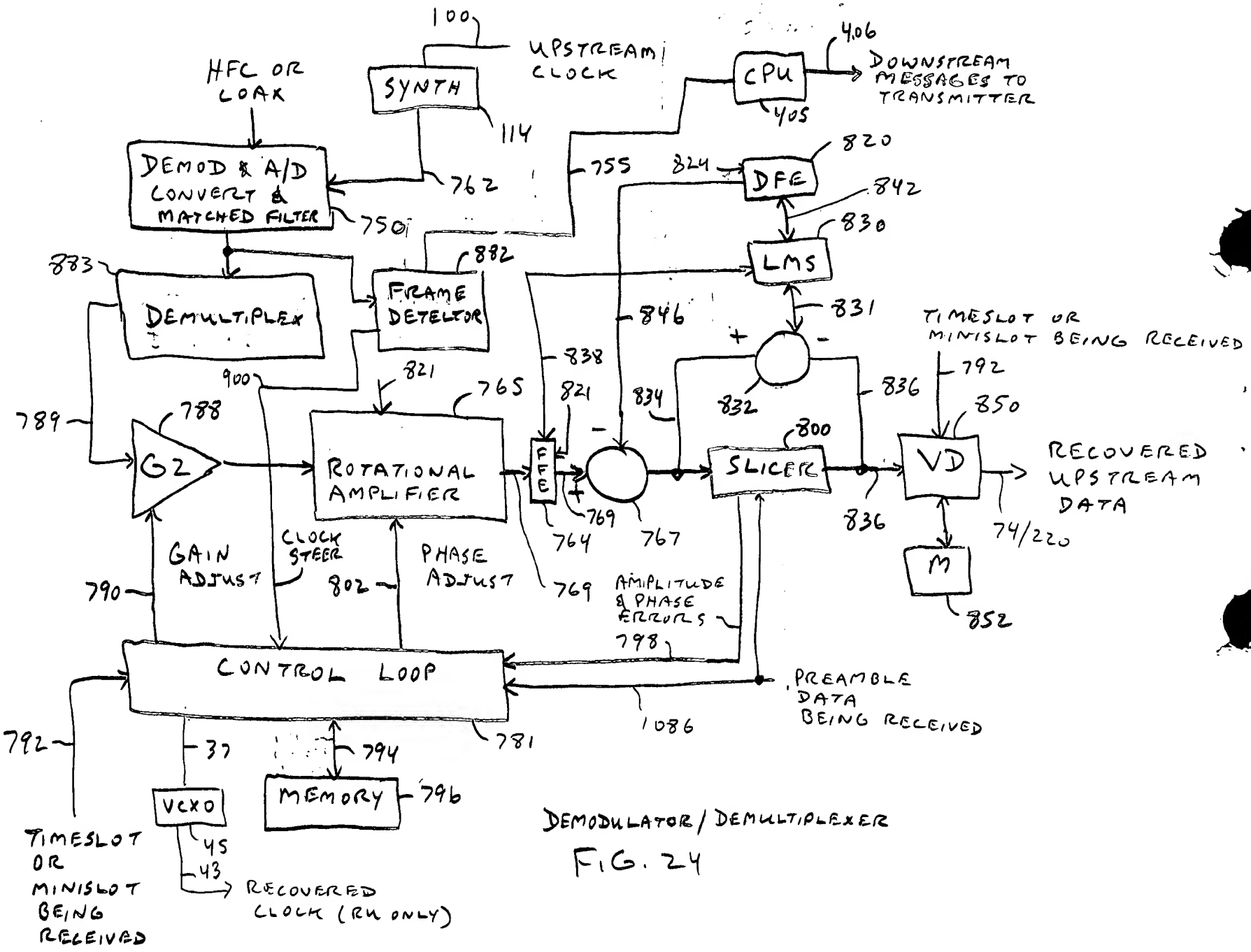


FIG. 23



DEMODULATOR / DEMULTIPLEXER

FIG. 24